INFORMATION DISCLOSURE CITATION

PTO-1449

Complete if Kn wn	
Application No.	~~Unknown~~ 10/684,637
Filing Date	10/14/2003
First Named Inventor	Nicholas D. Signore
Group Art Unit	~~Unknown~~ 2825
Atty. Docket No.	SUN-P9727-MEG

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
SB	6,629,301	Sep. 30, 2003	Sutherland *et al.*	716	8	Sep. 15, 2000

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation Yes	Translation No
						☐	☐
						☐	☐
						☐	☐

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

SB	Sutherland *et al.*, Logical Effort Designing Fast CMOS Circuits, 1999

EXAMINER	DATE CONSIDERED
Barbara Bowen	2/21/06

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.